Specification

Industrial Grade
1U Switching Power Supply
650W ATX Output Power
Universal AC Input, Active PFC

P/N: P8650I 1F

*** Specification Approval ***

This specification (total 13 pages including drawings) is approved in entirety by:

Company Name	Print Name	Signature	Date

Specification subject to change without prior notice.

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1. General

This is the specification of Model P8650I 1F. It is intended to describe the functions and performance of the subject power supply.
This 1U 650 watts switching power supply with Active PFC (Power Factor Correction) capability, meets EN61000-3-2 and equips Full Range Input features.

2. AC Input Specifications

2.1 AC Input Voltage, Frequency and Current (Rating: 100V-240Vac, 47-63Hz, 9-4.5A)

The power supply must operate within all specified limits over the input voltage range in Table 1. Harmonics distortion of up to 10% THD must not cause the power supply to go out of specified limits.

Parameter	Minimum	Nominal	Maximum	Max. Current
Voltage (115V)	90 Vac	100-120Vac	132 Vac	10A
Voltage (230V)	180 Vac	200-240Vac	264Vac	5A
Frequency	47 Hz	50 / 60 Hz	63 Hz	

Table 1 – AC Input Voltage and Frequency

2.2 AC Inrush Current

The power supply must meets inrush requirements of any rated AC voltage, during turn on at any phase of voltage, during a single cycle AC dropout condition, during repetitive On/Off cycling of AC, and over the specified temperature range. The peak inrush current shall be less than the rating of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

2.3 Input Power Factor Correction (Active PFC)

The power factor at full load shall be $\geq$ 0.95 at nominal input voltage.

2.4 Input Current Harmonics

When the power supply is operated in 90-264Vac of Sec. 2.1, the input harmonic current drawn on the power line shall not exceed the limits set by EN61000-3-2 class “D” standards. The power supply shall incorporate universal power input with active power factor correction.

2.5 AC Line Dropout

An AC line dropout of 16mS or less shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than 17mS the power supply should recover and meet all turn on requirements. The power supply shall meet the regulation requirement over all rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply. An AC line dropout is defined as a drop in AC line to 0VAC at any phase of the AC line for any length of time.

3. DC Output Specification

3.1 Output Current / Loading

The following tables define two power and current rating. The power supply shall meet both static and dynamic voltage regulation requirements for minimum load condition.

Output Voltage	+5V	+3.3V	+12V1	+12V2	+12V3	+12V4	-12V	+5VSB
Max. Load	25A	25A	18A	18A	18A	18A	0.8A	3A
Min. Load	1A	0A	0.8A	0.8A	0.8A	0.8A	0A	0.1A
Max. Combined	**180W**		**48A**					
Total Output	**630W**						**6W**	**15W**

Table 5 – Output Loads Range 1:

Note 1: Maximum continuous total DC output power should not exceed 650 W.

Note 2: Maximum combined load on +5V and +3.3V outputs should not exceed 180W.

Note 3: Maximum combined load on +12V1, +12V2 +12V3 and +12V4 outputs should not exceed 48A.

3.2 DC Voltage Regulation, Ripple and Noise

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. All outputs are measured with reference to the return remote sense (ReturnS) signal. The +5V,+3.3V, +12V, -12V and +5VSB outputs are measure at the power supply connectors references to ReturnS. The +5V and +3.3V is measured at its remote sense signal (+5VS, +3.3VS) located at the signal connector.

Output Voltage	+5V	+3.3V	+12V1	+12V2	+12V3	+12V4	-12V	+5VSB
Load Reg.	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-10%	+/-5%
Line Reg.	±1%	±1%	±1%	±1%	±1%	±1%	±1%	±1%
Ripple & Noise	50mV	50mV	120mV	120mV	120mV	120mV	120mV	50mV

Table 7 – Regulation, ripple and noise

Ripple and Noise shall be measured using the following methods:

a) Measurements made differentially to eliminate common-mode noise

b) Ground lead length of oscilloscope probe shall be ≤ 0.25 inch.

c) Measurements made where the cable connectors attach to the load.

d) Outputs bypassed at the point of measurement with a parallel combination of 10uF tantalum capacitor in parallel with a 0.1uF ceramic capacitors.

e) Oscilloscope bandwidth of 0 Hz to 20MHz.

f) Measurements measured at locations where remote sense wires are connected.

g) Regulation tolerance shall include temperature change, warm up drift and dynamic load

3.3 Timing Requirements

These are the timing requirements for the power assembly operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70mS. The +5V, +3.3V and +12V output voltages should start to rise at about the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 50 mS (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 mS (T_{vout_off}) of each other during turn off. Figure 1 and figure 2 show the turn On and turn Off timing requirement. In Figure 2, the timing is shown with both AC and PSON# controlling the On/Off of the power supply.

Item	Description	MIN	MAX	Units
Tvout_rise	Output voltage rise time from each main output.(+5Vsb < 70mS)	5	70	mS
Tvout_on	All main output must be within regulation of each other within this time.		50	mS
Tvout_off	All main output must leave regulation within this time		400	mS

Table 10 – Output Voltage Timing

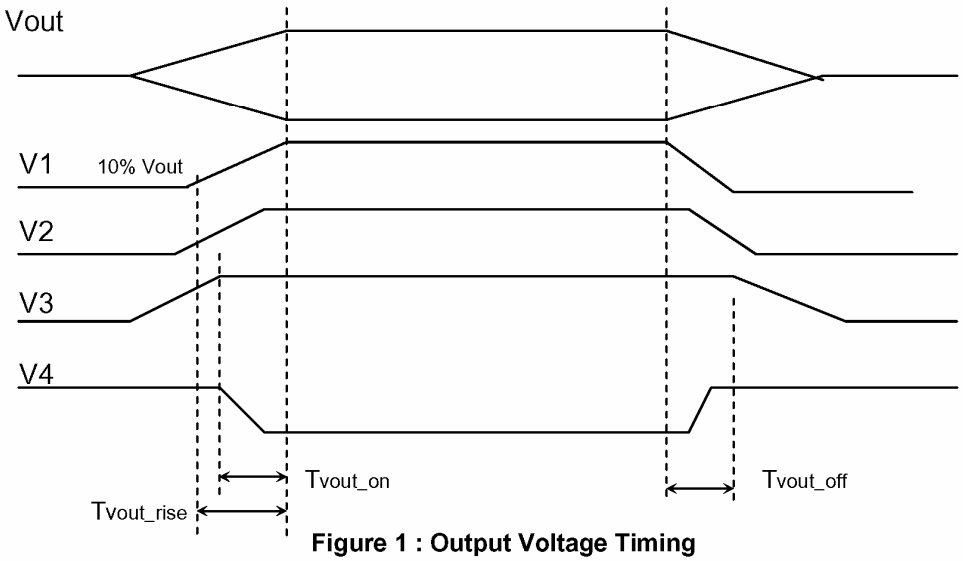

Figure 1 : Output Voltage Timing

Table 11 – Turn On/Off Timing

Item	Description	MIN	MAX	Units
Tsb_on-delay	Delay from AC being applied to +5VSB being within regulation.		1500	mS
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	mS
Tvout_holdup	All main output voltage stay within regulation after loss of AC	18		mS
Tpwok_holdup	Delay from loss of AC deassertion of PWOK.	17		mS
Tpson_on_delay	Delay from PSON# active to output voltage within regulation limits.	5	400	mS
Tpson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	mS
Tpwok_on	Delay from output voltage within regulation limits to PWOK asserted at turn on.	100	500	mS
Tpwok_off	Delay from PWOK deasserted to output voltages (+5V, +3.3V, +12V) dropping out of regulation limits.	1		mS
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON# signal. .	100		mS
Tsb_vout	Delay from +5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	mS

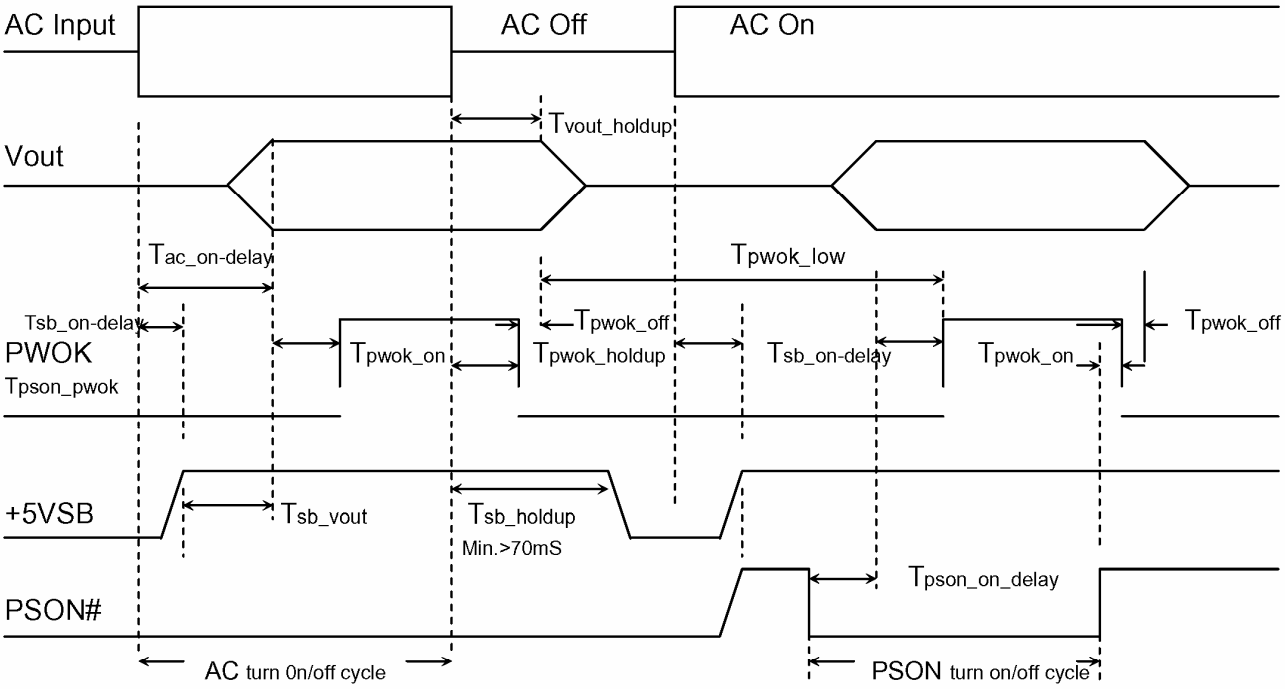

Figure 2 : Turn On/Off Timing

3.4 Remote On/Off Control : PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +5V, +3.3V, +12V and –12V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB and V bias) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to VSB locted in power supply.**
PSON# = Low	Power ON
PSON# = High	Power OFF

Table 13 – PWOK Signal Characteristic

3.5 Efficiency

The efficiency is specified at 50% and 20% loading conditions to help reduce system power consumption at typical system loading conditions.

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Loading	100% of minimum	50% of minimum	20% of minimum
Minimum	80%	80%	80%

3.6 +5VSB (Standby)

The +5VSB output is always on (+5V Standby) when AC power is applied and power switch is turned on.

The +5VSB line is capable of delivering at a maximum of 3A for PC board circuit to operate.

4. Protection

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, either a AC cycle OFF for 15 sec, or PSON# cycle HIGH for 1 sec must be able to restart the power supply.

4.1 Over Current Protection

This power supply shall have current limit to prevent the +5V, +3.3V, and +12V outputs from exceeding the values shown in table 14. The current limit shall not trip under maximum continuous load or peak loading as described in Table 5. The power supply shall latch off if the current exceeds the limit. The latch shall be cleared by toggling the PSON# signal or by cycling the AC power. The power supply shall not be damaged from repeated power cycling in this condition. The -12V and +5VSB outputs shall be shorted circuit protected so that no damage can occur to the power supply.

Voltage	Minimum	Maximum	Shutdown Mode
+5V	110%	150%	Latch Off
+3.3V	110%	150%	Latch Off
+12V	110%	150%	Latch Off

Table 14 –Over Current Protection

4.2 Over Voltage Protection

The power supply shall shut down in a latch off mode when the output voltage exceeds the over voltage limit shown in Table 4.

Voltage	Minimum	Maximum	Shutdown Mode
+5V	+5.74V	+7V	Latch Off
+3.3V	+3.76V	+4.3V	Latch Off
+12V1,2,3,4	+13.4V	+15.6V	Latch Off

Table 15 –Over Voltage Protection

4.3 Short Circuit Protection

The power supply shall shut down in a latch off mode when the output voltage is short circuit.

5. Field Replacement Unit (FRU)/ I²C Function

5.1 Field Replacement Unit (FRU) Signal

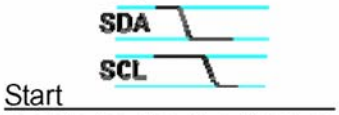
Two pins will be allocated for the FRU information on the power supply connector. One pin is the Serial CLOCK (SCL). The second pin is used for Serial DATA (SDA).

The FRU circuits inside the power supply must be powered off of 5VSB on the system side of the device and grounded to ReturnS (remote sense return). The Write Control (or Write protect) pin should be tied to ReturnS inside the power supply so that information can be written to the EEPROM.

5.2 I²C Bus Events: The START and STOP conditions

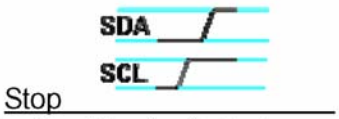
Prior to any transaction on the bus, a START condition needs to be issued on the bus. The start condition acts as a signal to all connected IC's that something is about to be transmitted on the bus. As a result, all connected chips will listen to the bus.

After a message has been completed, a STOP condition is sent. This is the signal for all devices on the bus that the bus is available again (idle). If a chip was accessed and has received data during the last transaction, it will now process this information (if not already processed during the reception of the message).



Start

The chip issuing the Start condition first pulls the SDA (data) line low, and next pulls the SCL (clock) line low.



Stop

The Bus Master first releases the SCL and then the SDA line.

5.3 SMBus protocols

Each message transaction on SMBus follows the format of one of the defined SMBus protocols. The SMBus protocols are a subset of the data transfer formats defined in the I^2C specifications. I^2C devices that can be accessed through one of the SMBus protocols are compatible with the SMBus specifications. I^2Cdevices that do not adhere to these protocols cannot be accessed by standard methods as defined in the SMBus and ACPI specifications.

5.4 Transferring Data: Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I^2C-bus format (for CBUS compatible devices for example). A message, which starts with such an address, can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated.

5.5 Transferring Data: Acknowledge

Data transfer with acknowledges is obligatory. The master generates the acknowledge-related clock pulse. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. Of course, set-up and hold times must also be taken into account.
Usually, a receiver, which has been addressed, is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function) the data line that must be left HIGH by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.
If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer.

The slave generating the not-acknowledge on the first byte to follow indicates this. The slave leaves the data line HIGH and the master generates a STOP or a repeated START condition.
If a master-receiver is involved in a transfer, it must signal the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

6. Environmental Requirements

6.1 Temperature

Operating Temperature Range:	0°C ~ 50°C (32°F~ 122°F)
	The rated power will derate from 100% to 80% for from 40°C to 50°C
Non-Operating Temperature Range:	-40°C ~ 85°C (-40°F~ 176°F)

6.2 Humidity

Operating Humidity Range:	20% ~ 90%RH non-condensing
Non-Operating Humidity Range:	10% ~ 95%RH non-condensing

7. Agency Requirements

7.1 Safety Certification.

Product Safety:	UL 60950-1 2000Edition, IEC60950-1, 3rd Edition EU Low Voltage Directive (73/23/EEC) (CB) TUV, CCC
RFI Emission:	FCC Part15 (Radiated & Conducted Emissions) CISPR 22,3rd Edition / EN55022: 1998 + A1: 2000)
PFC Harmonic:	EN61000-3-2:2000
Flicker:	EN61000-3-3: 1995 + A1: 2002
Immunity against: **-Electrostatic discharge:** **-Radiated field strength:** **-Fast transients:** **-Surge voltage:** **-RF Conducted** **-Voltage Dips and Interruptions**	EN55024: 1998 + A1: 2001 and A2: 2003 -IEC 61000-4-2 -IEC 61000-4-3 -IEC 61000-4-4 -IEC 61000-4-5 -IEC 61000-4-6 -IEC 61000-4-11

Table 16 –Safety Certification

7.2 AC Input Leakage Current

Input leakage current from line to ground will be less than 3.5mA rms. Measurement will be made at 240 VAC and 60Hz.

8. Connections

8.1 AC Input Connector

The AC input connector shall be an *IEC 320 C-14* power inlet. This inlet is rated for 15 A/250 VAC.

8.2 DC Wire Harness and Connector Requirements

(Subject to change without notice; please see appendix: wireharness drawing)

P1: Motherboard Power Connector

Connector housing: 24- Pin Molex 5557 (No.39-01-2240) or Equivalent

Contact: Molex 5556T (No.44476-1111) or Equivalent

Pin	Signal	Color	Size	Pin	Signal	Color	Size
1	+3.3 VDC	Orange	16 AWG	13	+3.3 VDC;+3.3VRS+	Orange / Brown	16 AWG/ 22AWG
2	+3.3 VDC	Orange	16 AWG	14	-12 VDC	Blue	18 AWG
3	COM	Black	18 AWG	15	COM	Black	18 AWG
4	+5 VDC	Red	18 AWG	16	PS_ON#	Green	22 AWG
5	COM	Black	18 AWG	17	COM	Black	18 AWG
6	+5 VDC	Red	18 AWG	18	COM	Black	18 AWG
7	COM	Black	18 AWG	19	COM	Black	18 AWG
8	PW_OK	Gray	22 AWG	20	N/C	--	--
9	5VSB	Purple	18 AWG	21	+5 VDC	Red	18 AWG
10	+12V3	Yellow/Blue stripe	18 AWG	22	+5 VDC ;+5V RS+	Red; Red	18 AWG; 22AWG
11	+12V3	Yellow/Blue stripe	18 AWG	23	+5 VDC	Red	18 AWG
12	+3.3 VDC	Orange	16 AWG	24	COM	Black	18 AWG

P2: Processor Power Connector (sectional connector 4-Pin + 4-Pin)

Connector housing: 8- Pin Molex 5557 (39-01-2080) or Equivalent

Contact: Molex 5556T (39-00-0059) or Equivalent

Pin	Signal	Color	Size	Pin	Signal	Color	Size
1	COM	Black	18 AWG	5	+12 VDC1	Yellow/Black stripe	16 AWG
2	COM	Black	18 AWG	6	+12 VDC1	Yellow/Black stripe	16 AWG
3	COM	Black	18 AWG	7	+12 VDC2	Yellow	16 AWG
4	COM	Black	18 AWG	8	+12 VDC2	Yellow	16 AWG

4-Pin HDD / CD-ROM Drive Power Connectors

Connector housing: 4- Pin AMP: 1-480424-0 or Molex 8981-04P or Equivalent

Contact: Amp 61314-1 or Equivalent

Pin	Signal	Color	Size
1	+12V4	Yellow/Green stripe	18 AWG
2	COM	Black	18 AWG
3	COM	Black	18 AWG
4	+5 VDC	Red	18 AWG

Small 4-Pin : Floppy Disk Drive Power Connectors

Connector housing: 4- Pin AMP: 171822-4 or Equivalent

Pin	Signal	Color	Size
1	+5 VDC	Red	22 AWG
2	COM	Black	22 AWG
3	COM	Black	22 AWG
4	+12 V4	Yellow/Green stripe	22 AWG

Serial ATA Power Connector

This is a required connector for systems with serial ATA devices.
Molex Housing #675820000 or Equivalent
Molex Terminal #67510000 or Equivalent

Pin	Signal	Color	Size
1	+12V4	Yellow/Green stripe	18 AWG
2	COM	Black	18 AWG
3	+5VDC	RED	18 AWG
4	COM	Black	18 AWG
5	+3.3VDC	Orange	18 AWG

9. Physical Characteristics Size

9.1 Power Supply Dimension: 100 mm(W) x 40 mm(H) x 275 mm(D)

Mechanical drawing: Please refer to the attached sketch.